

Low Power Design Industry Relevance

Freescale Semiconductor Inc.

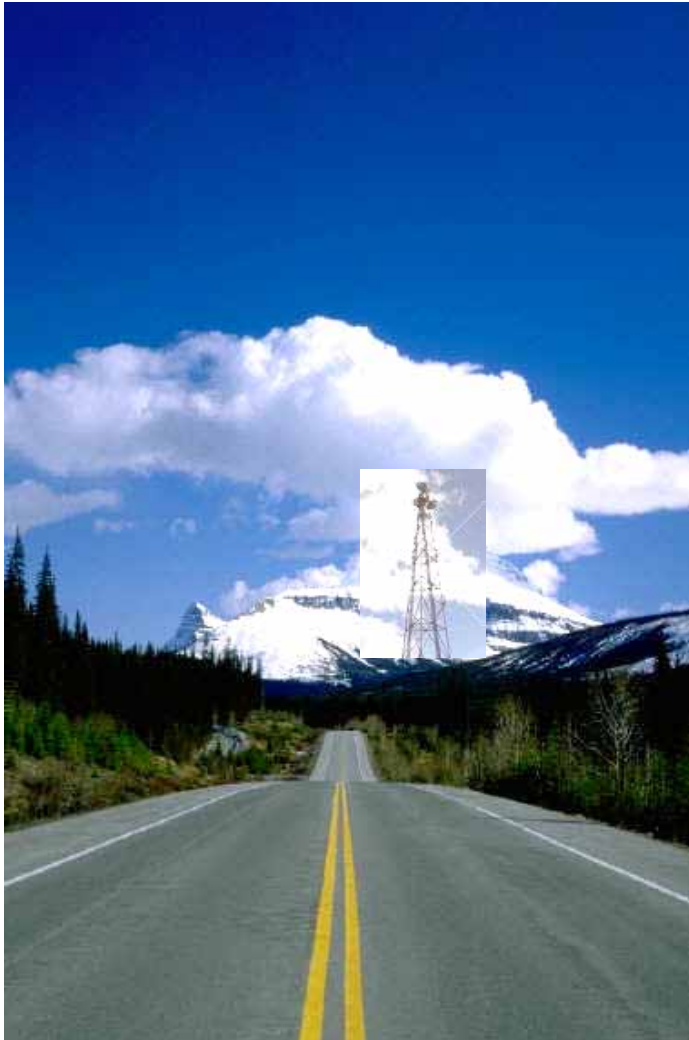
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Wireless Carriers



Low Power Design is absolutely critical and has a direct impact to carrier revenue.

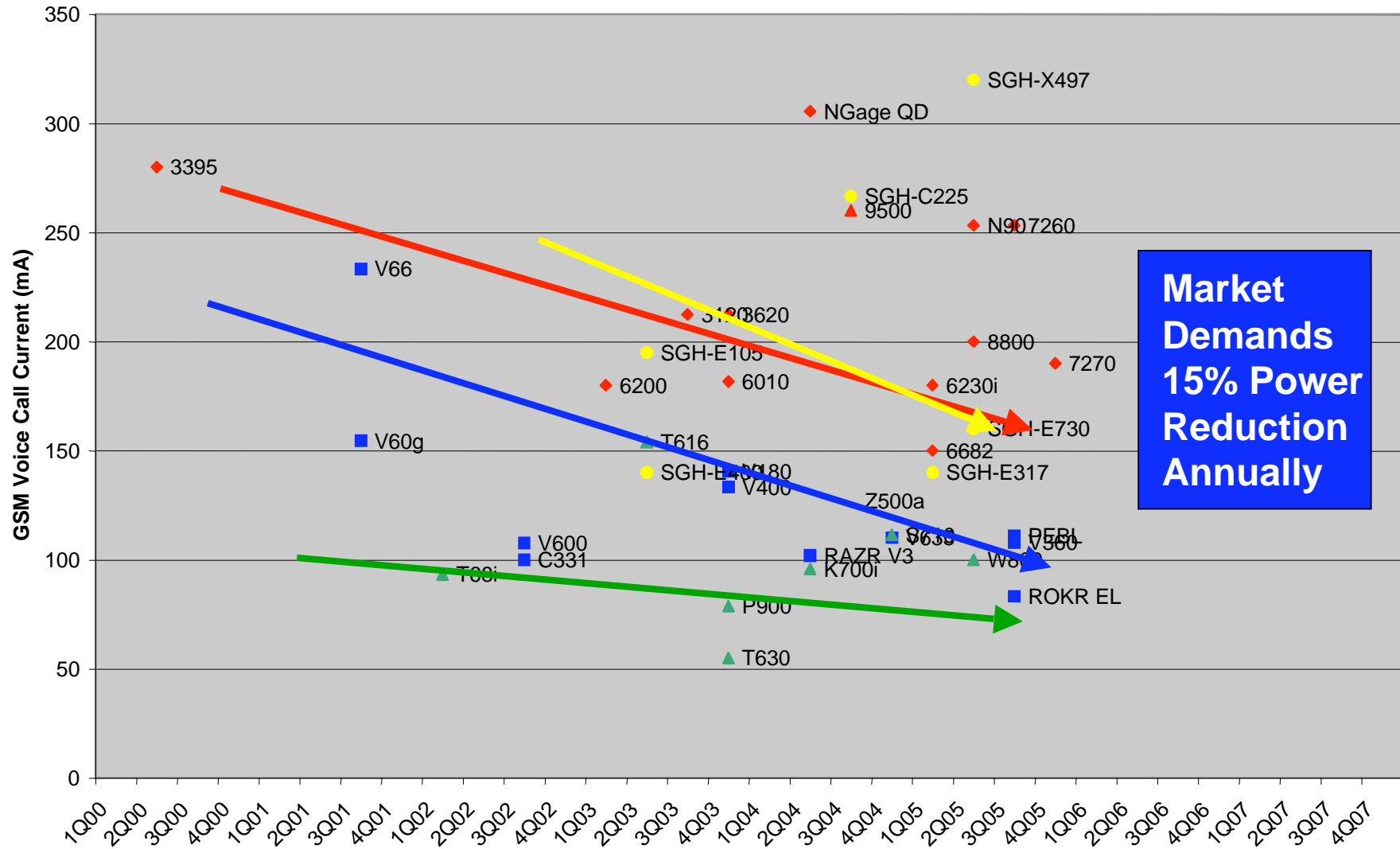
If the cell phone is powered off, The source of revenue is off for a carrier.

Performance needed to sell the phone. Power needed to bring revenue.

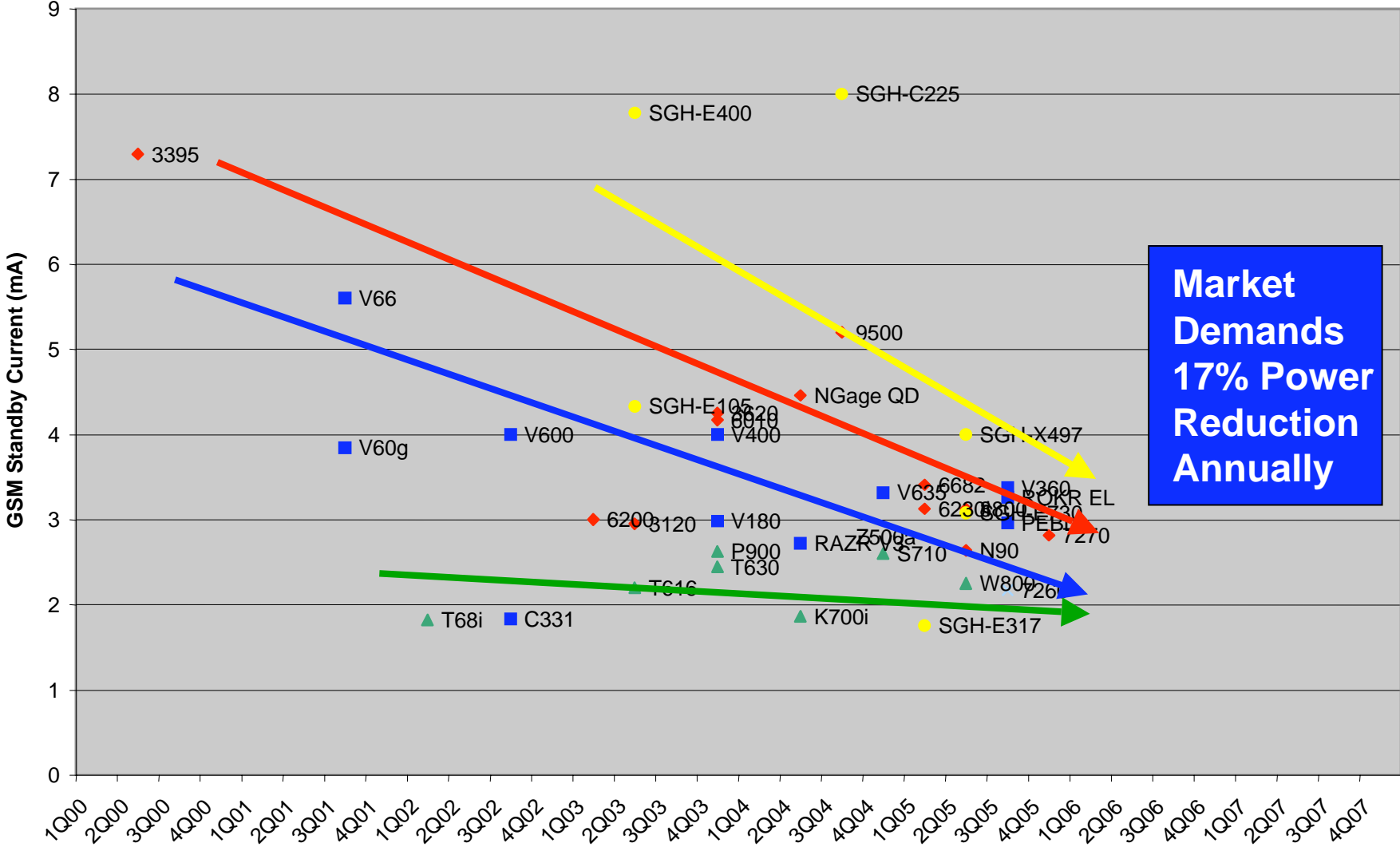
Wireless and Handheld Devices

- Standby and Talk time are the benchmark parameters for cell phone industry.
- MP3 playback time is benchmark for MP3 players and MP3 capable phones.
- These benchmark parameters are a direct reflection of battery and power consumption
- Speed is not a tradeoff factor for power.
- Power Performance ratio must be very high.
- Consumers are becoming power aware and can make intelligent and smart choices.

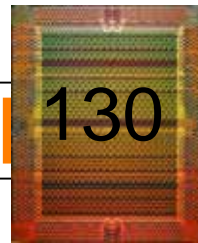
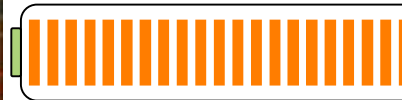
GSM Phone Talk Power



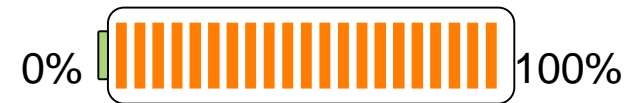
GSM Phone Standby Power



Energy consumption doubles with move from 130 to 90nm



Battery Power



Energy consumption doubles with move from 130 to 90nm



Battery Power



Battery Power

Leakage power: at 65nm, standby power is nearly half of the operating power



Energy



Goal: Extend Phone Battery Life

- Battery life is proportional to energy consumed
- Energy is power consumed over time
- Wireless designers must manage energy consumption.

To extend battery life, designers must minimize active and leakage power.

Hierarchical view of Energy Conservation

**Software
Definitions**

Dynamic system monitoring and intelligent control of energy saving

**Platform
Definitions**

Power Trees, Connectivity of components & consistent platform power modes

**Architectural
Definitions**

Heterogeneous processing resource optimization: MCU, DSP, accelerators, functional processing units

**Design
Definitions**

Hardware support for power gating, low-power idle modes, SRPG, AWB, DVFS, DPTC, Biasing techniques

**PROCESS node
Definitions**

Transistor design, Vt Optimization, memory bitcell design. Special circuits, libraries, custom and analog blocks

Problem Perspective

System Level

Software Definitions

Dynamic system monitoring and intelligent control of energy saving

Platform Definitions

Power Trans...
... modes

Architectural Definitions

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Design Level

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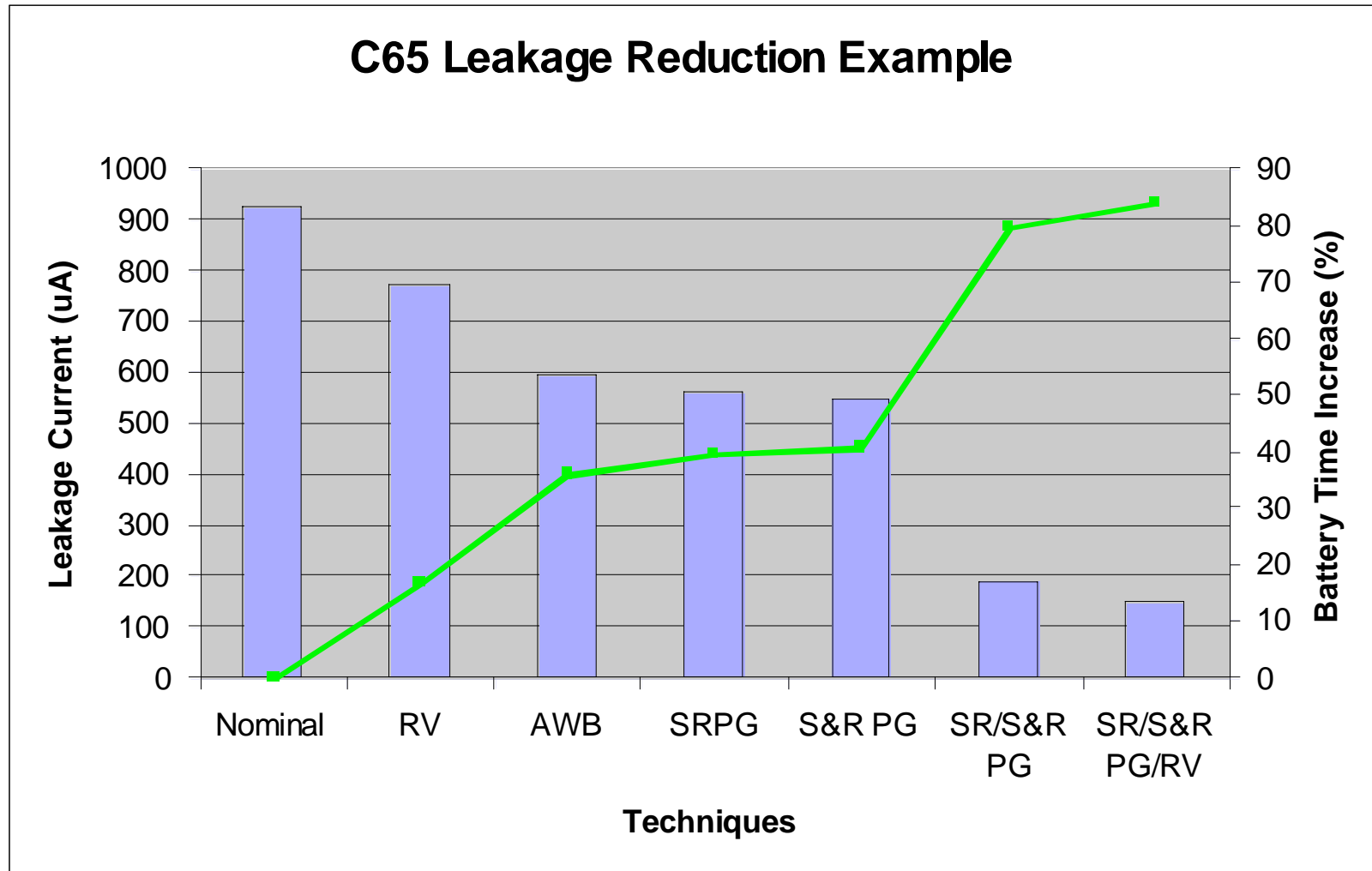
Low Power Design Needs

- Support Low Power Design Techniques thru the entire design flow using a single file format.
 - Design Representation
 - > Accurately define and capture the low power design intent, modes and constraints.
 - Design Implementation
 - > Floorplan and power grids.
 - > Common constraints for all tools (Synthesis, APR, timing, DFT)
 - > Design analysis tools with single power constraints.
 - > Accurate power estimation and measurements
 - Design Verification
 - > Voltage oriented simulators
 - > Various static power technique modeling and simulations.
 - > Silicon validation and correlation.

Static Power Design

- Static Power is crucial for defining standby time of cell phone.
- Multiple Leakage Reduction Techniques
 - Active Well Biasing (AWB)
 - State Retention Power Gating (SRPG)
 - Save and Restore with power gating. (S&R PG)
 - Multi-Vt based design styles
 - Aggressive Voltage Reduction during standby mode (RV)
 - Device biasing.
 - Switches, Isolation collars and level shifters.
- Static Power a big part of active power
 - Use switches for power mode switching.
 - Thermal dissipation issues in packaging.

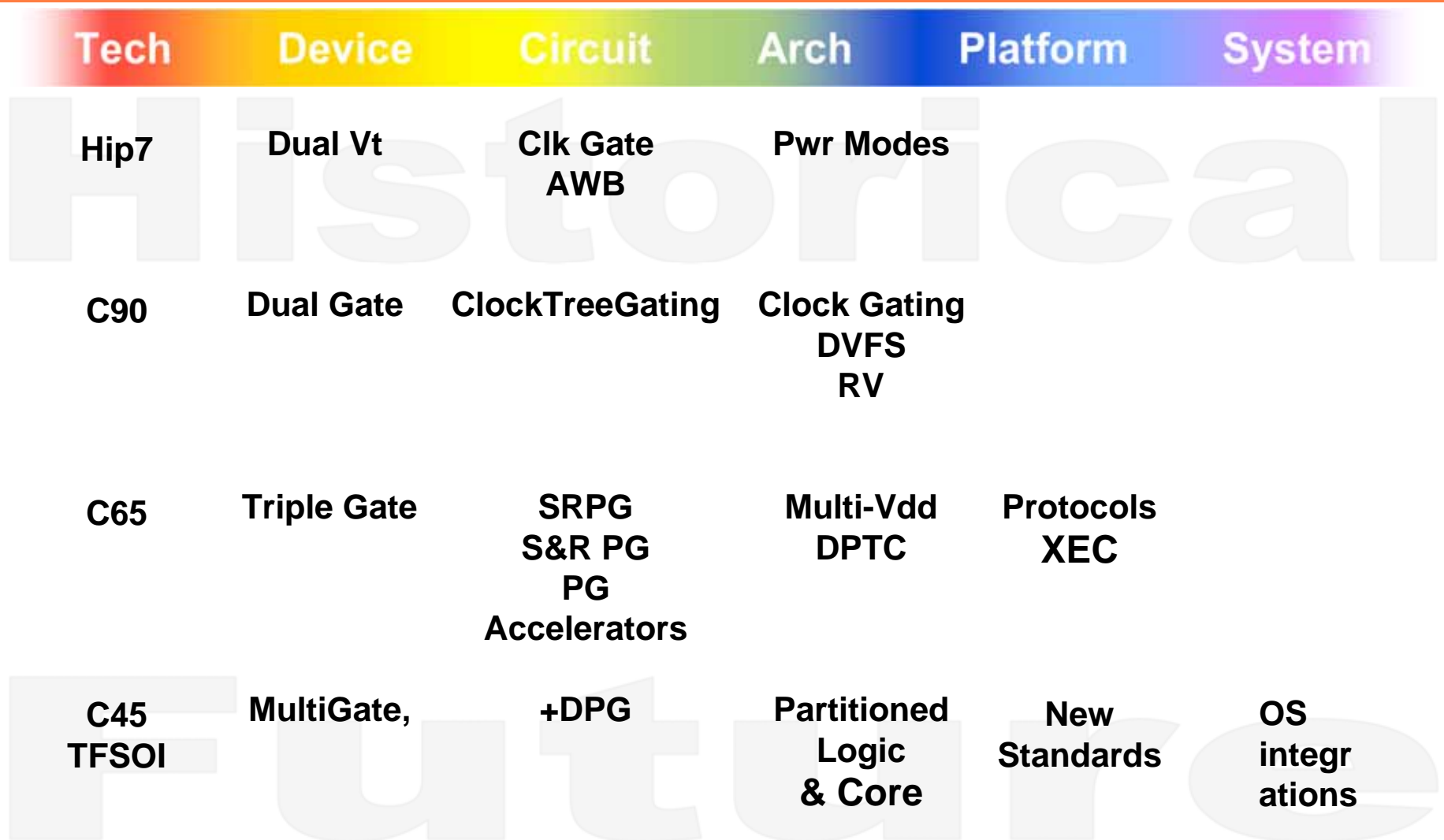
Example Leakage Reduction Techniques



Multi Voltage Design Styles - DVFS

- Voltage partitioning decisions are crucial and very key for power performance factor.
- Clear statement of power nets and domains.
- Clocking is the major challenge for multivoltage designs. Need intelligent clock tree builders.
- Globally Asynchronous Locally Synchronous (GALS) design styles for efficient voltage partitioning.
- Asynchronous protocols to enable efficient voltage partitioning.
- SoC/IP and EDA infrastructure gear up for this requirement.
- Libraries and Memories optimization and modeling at multiple corners.
- Tools must understand multi corner analysis and optimization.

Power Reduction Technology Map



System Level Model

- Need a smooth handoff between various stages.
 - Platform and regulator connectivity
 - System efficiency
 - Power models
 - Platform power modes
- Majority of design level work should be reusable at system level.
- Consistent style across all levels of power problem.

