



Designers of sub-100nm chips who are worried about power consumption look almost certain to be forced to make a choice between two standards as a merger between them looks less likely than ever. Yet, behind the scenes, both standards are acquiring features from each other. By **Chris Edwards**

Dennis Brophy, vice chairman of electronic design automation standards body Accellera, underlined why power is at the top of the minds of many of those involved in the chip-design business: "Power has become a dominant issue. Up to 100nm, it was dominated by clock switching. Under 100nm it is leakage."

At a workshop held at the Design Automation and Test in Europe (DATE) conference held in Nice in mid-April, Mika Naula, a technology manager at

Nokia's research centre, said power has moved from being a lower priority for chip designers than performance and area to being one of the most important problems to be solved thanks to the explosion of gate counts in the move to the 65nm process node.

The change in priorities focused a lot of minds in design automation. Cadence Design Automation started work on its low-power initiative in 2005, an effort that led in November to the formation of the Low-Power

Coalition (LPC) of the Silicon Integration Initiative (SI2) standards body and, earlier this year, version 1.0 of the Common Power Format (CPF).

Accellera kicked off its own effort in the summer of last year and delivered version 1.0 of its own Unified Power Format (UPF) just nine months later. Shortly before the two standards were published, people working in the two said they believed a merger between the two was possible.

"In fact, that was probably one of the outcomes we expected out

of UPF," said Yatin Trivedi, director of product marketing at Magma Design Automation. The decision by three out of the four top design-automation companies to deliver a competing standard could have convinced Cadence that it was worth pushing for a merger. "Instead they went the other way," said Trivedi. "That has created a more dedicated from all of us and other vendors are now lining up with us."

Cadence is convinced that it has the momentum. "There is a

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lot of industry support around the Common Power Format," said Pankaj Mayor, group director at Cadence, adding that the foundries TSMC and UMC had agreed to adopt CPF for the next versions of their reference flows.

Although several companies have joined the LPC since its formation in November 2006, some of the founding group have since left. The leavers include design-tool suppliers Magma and Synopsys as well as leading chipmaker Texas Instruments. However, since the formation of the LPC, AMD, Freescale Semiconductor and IBM have joined the group.

#### TWIN TRACKS

Many of the companies in the LPC have taken part in the UPF effort. Accellera claimed that LPC participants AMD, Freescale, IBM, Intel, LSI Logic, NXP Semiconductors, STMicroelectronics and TI have also contributed to the UPF process.

By early May, a IEEE working group was formed to take the Accellera work and, potentially merge what has been produced by the LPC into a single standard. Brophy said the process to define an IEEE standard based on UPF could be quite quick, with an approved standard by the end of the year being possible.

Referring to Cadence, Brophy said: "We are talking to see whether we can use IEEE to converge the one holdout. I am not fighting. We are talking to

determine points of collaboration. There is a lot of history of collaboration. And we continue to have discussions with them in the low power area."

By June, a merger did not look any more likely than it did when the IEEE study group pushed for a power-definition standard around UPF. Both the LPC and Accellera held parallel sessions at the Design Automation Conference (DAC) in San Diego to explain their progress to chip designers.

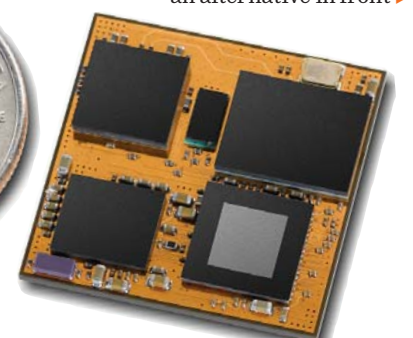
Jan Willis, senior vice president of industry alliances at Cadence, said a move to deliver CPF to the IEEE to produce a combined standard is possible. "It is in the hands of the LPC," she said, but added that Cadence did not favour taking the format to the IEEE in the way that Accellera has proposed. "We don't see it as workable, although Cadence is just one voice. It is not just about a format."

Willis claimed that Cadence "did everything we could" to bring about a single standard. "We sat down with people in June of last year and asked, 'what do we need to do for you to be comfortable with this?'" She said the other major tools vendors chose to stay with the Accellera process rather than join in the SI2-sponsored project.

Trivedi countered: "There were opportunities for Cadence to come in and donate CPF. It could have been the end of the problem and Cadence chose not to do it. That was what brought UPF."

Despite the differences between members of the two competing groups, there may yet be a convergence of sorts. If the LPC decides not to join, there is an alternative in front ▶

Wireless designs such as RF modems will use the new power formats



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## THE PROPOSALS SEPARATED AT BIRTH

For all the infighting, the two power-definition formats are not all that different. They are even based on the same core language.



The proposed standards are still young and similar, even as committees iron out the bits that do not match up

The backbone of both the CPF and UPF standards is the tool control language (Tcl). This is a scripting language originally created to provide a way to automate the control of physical-layout software and turns up in a number of electronic design automation tools.

The attraction of Tcl is that command-line commands can be used as statements in a script – there is no need to embed them as function calls as you would have to using C. Most Tcl implementations are specific to an individual tool. The CPF and UPF definitions are unusual in that they are meant to be used with all tools in a power-aware flow – the tools work out whether the commands supplied in the Tcl are relevant to them or not.

The functions of CPF and UPF overlap a lot, with omissions and

differences on either side. For example, both formats use the same command "create\_power\_domain" to define a set of blocks in the design that can be powered differently to other blocks on the same chip. However, the power supplies that provide energy for a domain are defined using different directives – "create\_power\_nets" in CPF and "create\_supply\_net" in UPF. They have more or less the same effect.

The idea behind both formats is that power-aware tools read in the description of which blocks in a design can be powered up and down independently. The tools can use that information to determine, for example, how a simulation will behave under different powering conditions.

For example, a testbench

written in SystemVerilog may identify to the simulator that a particular block should be powered down to ensure that other blocks do not access it without checking on power status first. It does that by referring to the name of a domain created in the Tcl power-description file.

A transistor-level simulation may use the power definitions to see what happens when supply voltages or substrate bias voltages change. Does all the necessary logic paths meet expected timing when the supply voltage to one block is lowered to save power while others are running at their maximum voltage? Or a static analysis tool may check that the correct level shifters are in place to ensure that blocks in different power domains can communicate.

of Accellera and the proposed IEEE working group: simply incorporate elements that users like in CPF but which are not yet in UPF and then let the market decide which syntax it prefers.

"NXP, LSI and other companies that had been working SI2, they have a difference document," Brophy explained. "They brought that document to show things that are missing [in UPF compared with CPF]: could we address these issues? I think what we can end up with is a converged version."

### GAP FILLING

A similar approach is open to the LPC and, there are some elements of the UPF work that are likely to be adopted by CPF users even if the coalition itself does not accept them. Vic Kulkarni, CEO of Sequence Design, a member of the LPC, said the group has to build on the existing version to keep pace with the industry. "We need to give users a continuous approach to adopting new techniques and methods," he said.

Kulkarni said CPF is currently missing a way of describing clock-gating strategies and should adopt a file format developed by Synopsys that was then donated to Accellera and employed in UPF. This is the switch activity interchange format (SAIF).

Magma's Trivedi explained that SAIF is important in low-power flows because it provides a way to define how logic in a block will switch to give an idea of the density of transitions under different circumstances, letting tools estimate power consumption.

Trivedi explained that, before SAIF, the value change dump (VCD) file format used by simulators to produce waveform diagrams had to be used. "It was not the most efficient way of doing things. But, with Synopsys opening up SAIF, it was made much easier for everybody," he said.

Mitch Dale, product marketing director for Calypto Design Systems, like Sequence a member of the LPC rather than a participant in UPF, agreed with



Freescale Semiconductor has adopted CPF to help drive its verification processes for low-power systems

Kulkarni that SAIF support would be useful in CPF: "We see SAIF as being a pretty well used interface. Most customers have that so we support it. We are looking at supporting any standards that exist: as a startup we have to fit into design flows."

However, there will be important points of divergence between CPF and UPF if the two efforts do not merge formally. Willis criticised the use of

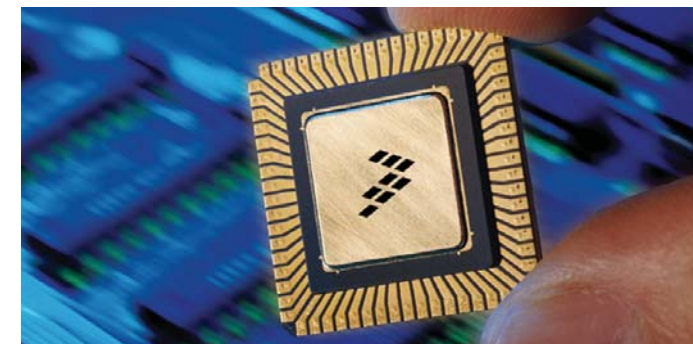
Synopsys's Liberty library format in UPF. "Is that an open standard? It is still all owned and decisions are made by Synopsys," she said.

The next phase of development will see users put the flows built on CPF and UPF into action, with vendors choosing either to back just one of the formats or basing their tools on a neutral format and then using translators to let them deal with other products.

"You will find a few differences between the formats at the technical level. But the differences are 98% political, 2% technical," said Trivedi.

Processor-core supplier ARC has backed CPF. "We have embarked on this road of low-power design flows in partnership with Cadence," said Colin Holehouse, senior engineer at ARC, but he said that, as an IP supplier, the company may need to have links to UPF. "It will be a pain to deal with two standards. But, our intention is to encode the power intent into a neutral form and use that to configure the low-power reference flows that we support."

Dave Gross, low-power manager at Freescale, said his company has decided to use CPF because Cadence is the primary supplier of chip-design tools for the groups currently interested in power-saving techniques.



"The ones pushing UPF are not really our primary vendors," he said. "The area that may be affected by this is maybe transportation, where there is some use of VHDL. We would have to kind of convert between formats in that case. But this effort is at such an early stage it is not really an issue now."

Gross said Freescale is moving to the third phase of development with CPF, moving to a live project from pilot projects that took designs with power-saving modes defined using the format almost to tape-out.

Those users who need translation between CPF and UPF are likely to be able to find support. Atrenta is building support for both formats into its SpyGlass Power tool, expecting the support to be ready by 2007, according to Michael Carrell, who is responsible for the marketing of Atrenta's power-analysis tools.

### FOUND IN TRANSLATION

"We are in the process of building a translator that can handle both UPF and CPF. Initially, our plan is to provide this to our customers so they have a path from either of these formats into SpyGlass Power and vice versa," Carrell said.

Gross said the ultimate winner will emerge in the marketplace, maybe not just for defining power intent but who provides the whole design flow: "The customers will be the ultimate definer of what is good and what is bad. This issue is becoming a microcosm of the macrocosm of the flows becoming so complex that you are pushed to adopt the flow from a primary vendor."

However, there are users who believe that cross-industry standards will be needed so they are not locked into one vendor's flow. "You need an integrated flow to do design efficiently," said Ralph van Vignau, senior director of infrastructure and standards at NXP. "But you need a flow that is flexible. If you have something with lots of RF on it, you need different ways of doing things than if you are just building a digital chip." ■